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| 10/006,511 | 12/05/2001 | Francis Edward Noel JR. | RAL920000108US1 | 8028 |

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| EXAMINER | |
|---|---|
| AHMED, SALMAN | |

| ART UNIT | PAPER NUMBER |
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| 2616 | |

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/006,511 | NOEL ET AL. | |
| | Examiner | Art Unit | |
| | Salman Ahmed | 2666 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12/5/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-21 are pending

Claims 1-21 are rejected.

### *Claim Rejections - 35 USC § 112*

1. In claim The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 1 recites the limitation "said physical layer devices" in line 11. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 6, 9, 10, 13, 14 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Cassing (C6x solutions for voice over IP gateway, Northcon/98 Conference Proceedings 21-23 Oct. 1998 Page(s):74 – 85).

In regards to claim 6, Cassing anticipates a network processor (figure 4) comprising: an embedded processor complex (EPC) with multiple processors (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner); a first communication interface to physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet), a second interface to a switch fabric (figure 4, T8100 Time Slot Interchange (TSI) switch); a memory storage unit (figure 4, SDRAM); a digital signal processor (DSP) (figure 4, TMS32OC6201 DSPs) having an analog I/0 (page 77, 2nd paragraph, DSPs perform Fax demodulation functions) and a digital I/0 interface (page 77 table 1, Serial port forms a glue-less interface to TDM frames); and a bus system for coupling said EPC, said physical layer devices, said switch fabric, said storage unit and said DSP (figure 4, shaded bus connection connecting various modules and page 74, section: *Gateway Architectural Requirements* Fast Arbitrated Bus: A high-speed bus for communications among modules).

In regards to claim 13 Cassing anticipates a method for improving the performance and functionality of a network processor (figure 4, i960 IOP and page 74,

section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner) controlling the communication between physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet) comprising the steps of: adding a DSP core (figure 4, TMS32OC6201 DSPs) to network processor (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner); coupling digital signals (page 77 table 1, Serial port forms a glue-less interface to TDM frames) to and from said network processor and said DSP; executing instructions by said DSP to determine a characteristic of said digital signals (page 76, last paragraph, the DSP subsystem is the most computationally intensive part of the voice gateways. The DSP subsystem hosts the following functions. Group 3 Fax Modems, Echo Cancellers, Voice encoder and decoders such as ITU-T standard speech coders Telephony signaling tone generators and detectors and HDLC processing for LAPD signaling); and directing a dispensation of digital signals based on said determined characteristic (page 77, last paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets. The i960 IOP, performs the function of routing the packets to the PCI bus. The IOP acts as a host for networking protocols. The IOP can also access the TDM signals via the HDLC controller. The HDLC controller allows access to HDLC formatted frames from WAN traffic).

In regards to claim 9, Cassing anticipates DSP (figure 4, TMS32OC6201 DSPs) is a functional core external (see figure 4) to EPC (figure 4, i960 IOP and page 74, section: *Gateway Architectural Requirements,* Protocol Processors: Possibly several embedded processors for hosting networking protocols in fault-tolerant distributed manner), DSP coupled to EPC and to one of physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet).

In regards to claims 10 and 19 Cassing anticipates DSP has an analog signal interface (page 77, 2nd paragraph, DSPs perform Fax demodulation functions) for receiving and sending analog signals and a digital signal interface (page 77 table 1, Serial port forms a glue-less interface to TDM frames) for sending and receiving digital signals.

In regards to claim 14, Cassing anticipates coupling analog signals (page 77, 2nd paragraph, DSPs perform Fax demodulation functions) to DSP; digitizing analog signals (page 77 second paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets); processing digitized analog signals by DSP (page 77 second paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets); incorporating processed digital signals into data packets corresponding to a communication protocol (page 79, 1st paragraph, Efficient canned support for TDM buffering, packetized speech. Low delay jitter buffer for pacektized speech), and receiving and transmitting data packets of processed digital signals to physical layer devices on a communication network coupled

to network processor (page 77, last paragraph, DSPs perform the speech encoding and Fax demodulation functions and form compressed packets. The i960 IOP, performs the function of routing the packets to the PCI bus. The IOP acts as a host for networking protocols. The IOP can also access the TDM signals via the HDLC controller. The HDLC controller allows access to HDLC formatted frames from WAN traffic).

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravindranath et al. (US PAT 6987756), hereinafter referred to as Ravindranath in view

of Wolf et al. (Design Issues for High-Performance Active Routers, Selected Areas in Communications, IEEE Journal on Volume 19, Issue 3, March 2001 Page(s):404 – 409).

Ravindranath teaches circuit for data communication comprising: circuitry (figure 3a, a telephone interface 310) for receiving digital signals from devices within a communication network (column 8 lines 64-66, If the endpoint is a digital telephone or equivalent, the telephone interface 310 is a digital telephone interface); circuitry (figure 3a, a telephone interface 310) for receiving analog signals from a selected one of said devices (column 8 lines 61-63, If the endpoint is an analog telephone or equivalent, the telephone interface 310 is an analog telephone interface), circuitry (figure 3a, processor 345) for routing (column 9 lines 38-41, the processor 345 controls the compression algorithm to be used by the DSP/CODEC 315, the protocol of the media, etc.) analog and digital signals to a digital signal processor (DSP) (figure 3a, the DSP/CODEC 315), the DSP outputting processed signals (column 9 lines 1-7, the DSP/CODEC 315 converts analog signals into a digital bit stream on bus 325 (in the case of an analog interface), or converts a digital input into a digital bit stream on bus 325 (in the case of a digital interface) using one of a number of compression algorithms) in response to DSP programming commands (column 9 lines 38-41, the processor 345 controls the compression algorithm to be used by the DSP/CODEC 315), circuitry (figure 3a, conversion module 330) for incorporating particular processed digital signals into data packets corresponding to a communication protocol (column 9 lines 7-12, the digital bit stream on bus 325 is received by a conversion module 330, which converts the bit

stream into packets, cells, etc. depending on the format selected by the terminal gateway 300); and circuitry (figure 3a, network interface module 335) for receiving and transmitting data packets of a communication protocol to and from a network coupling physical layer devices (column 9 lines 14-17, the network interface module 335 includes input/output first-in first-out devices (FIFOs), a transceiver, and timing circuits for transmitting packets, cells, etc. on the network cloud. Packets, cells, etc. received from the network cloud propagate in the opposite direction).

Ravindranath does not explicitly teach the circuit being an integrated circuit (IC).

Wolf in the same field of endeavor teaches multiple network processors with cache and memory on a single application specific integrated circuit are used to overcome the limitations of traditional single processor systems (Abstract).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ravindranath's system by incorporating it in an integrated circuit as taught by Wolf. The motivation is that (as suggested by Wolf, abstract; page 404, first column 2nd paragraph; conclusion) multiple network processors with cache and memory on a single application specific integrated circuit are used to overcome the limitations of traditional single processor systems. At the same time, continuing advances in integrated circuit technology are making it possible to implement several complete processor subsystems on a single chip. Such method provides a useful basis for extrapolation, as underlying IC technologies continue their inexorable progress to ever smaller geometries and higher performance levels.

In regards to claim 2, Ravindranath teaches circuitry for outputting analog signals derived from particular ones of processed signals from DSP to a particular one of physical layer devices (column 9 lines 17-21, Packets, cells, etc. received from the network cloud propagates in the opposite direction. In the case of media, the packets, cells, etc. propagate through the conversion module 330, DSP/CODEC 315, telephone interface 310, and to the appropriate endpoint).

In regards to claim 3, Ravindranath teaches DSP receives digital data not derived from a corresponding analog signal (column 8 lines 64-66, If the endpoint is a digital telephone or equivalent, the telephone interface 310 is a digital telephone interface).

In regards to claim 4, Ravindranath teaches selected first digital data from d DSP are analyzed by a network processor to determine a characteristic of first digital data, characteristic used in network processor to direct a dispensation of first digital data (column 9 lines 47-60, the DSP/CODEC 315 and/or telephone interface 310 forward signaling messages or commands received from the endpoint(s) to the endpoint message stack (e.g., off-hook, dialing, pressing transfer key, etc.) for processing by the processor 345. The processor 345 also sends commands to the DSP/CODEC 315 and/or telephone interface 310 for providing call processing functions to the endpoint (e.g., dialtone, ring, ringback, busy, etc.). The network interface module 335 and/or conversion module 330 forward messages received from telephony servers to the server message stack for processing by the processor 345 (e.g., dialtone message). The processor 345 sends messages to the conversion module 330 and/or the network

interface module 335 for transmission to the telephony servers (e.g., off-hook message)).

In regards to claim 5, Ravindranath teaches processing to determine characteristic of first digital data comprises a pattern recognition algorithm (column 9 lines 27-29, the processor 345 detects an off-hook signal from the telephone interface 310).

4. Claims 7, 8, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cassing in view of Chan et al. (US PAT 6826177), hereinafter referred to as Chan.

In regards to 7, 8, 16, 17 and 18 Cassing teaches using DSP and processors for implementing network communication as described in the rejections of claims 6 and 13 above.

In regards to 7, 8, 16, 17 and 18 Cassing does not explicitly teach DSP is one of multiple processors in EPC and DSP is a functional core integrated into each one of multiple processors in EPC.

Chan in the same field of endeavor teaches a packet telephony appliance having a network processor that integrates networking and DSP functions (column 1 lines 51-53).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Cassing's system by incorporating the concept of integration of

dsp within processors as taught by Chan. The motivation is that (as suggested by Chan, column 11 lines 46-49) such system is based on the Euphony network processor that integrates networking and DSP functions to provide a low cost and efficient solution for building networked appliances.

In regards to 18 Cassing teaches DSP coupled to one of physical layer devices (figure 4, J5 physical interface and page 74, section: *Gateway Architectural Requirements,* LAN I/O: Local Area Networking support. Typically 10/100 BaseT Ethernet).

5. Claims 11, 12, 15, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cassing in view of Ravindranath.

Cassing teaches doing message processing using DSP as described in the rejections of claim 6 above.

Cassing does not explicitly teach Dsp receives program commands via switch fabric from a remote device and receives program commands via a general-purpose processor in network processor.

Ravindranath in the same field of endeavor teaches the processor 345 controls the compression algorithm to be used by the DSP/CODEC 315, the protocol of the media, etc. (column 9, lines 38-40). Ravindranath in the same field of endeavor further teaches the DSP/CODEC 315 and/or telephone interface 310 forward signaling messages or commands received from the endpoint(s) to the endpoint message stack

(e.g., off-hook, dialing, pressing transfer key, etc.) for processing by the processor 345 (column 9 lines 47-51).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Cassing's system by incorporating the concept of dsp receiving commands from network and processor as taught by Ravindranath. The motivation is that by having dsp taking some of the processing responsibility from the processor via receiving commands from the network and processor, dsp will leave processors free to do other processing thus making the system robust.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571)272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 2616

SA
03/19/2006

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